REMARKS

The remainder of this Amendment is set forth under appropriate subheadings for the convenience of the Examiner.

1. Status of the Claims

Claims 1 through 21 are pending in the instant patent applications. Claims 1, and 10 are independent. Claims 2 through 9, and 19 through 20 depend from Claim 1. Claims 11 through 18 depend from Claim 10. New Claim 21 depends from Claim 1. Support for new Claim 21 can be found at various locations of the Applicant's specification, for example at FIG. 4, and at page 5, line 25 to page 6, line 4. Entry of the amendment is requested.

2. Rejection of Claims 1, 10, 19-20 under 35 U.S.C. § 103(a)

In the Action, the Office rejects Claims 1, 10, and 19-20 under 35 U.S.C. § 103(a) as being unpatentable over United States Patent Application Publication No. US 2002/0054005 A1 to Edwards *et al.* (hereinafter "Edwards") in view of newly cited United States Patent Application Publication No. US 2003/0146896A1 to Sekine (hereinafter "Sekine"). Applicant respectfully traverses the rejection by stating neither Edwards, Sekine, nor the combination thereof disclose or suggest all of the elements of the independent claims. Moreover, one skilled in the art would not be motivated to modify the teaching of these references, or their combination, to thereby obtain Applicant's invention.

a. Discussion of Applicant's Claims

Claim 1 recites a data scanner for driving a liquid crystal display (LCD). The data scanner includes a data bus containing digital data, and a row buffer coupled to the data bus for receiving and distributing the digital data received from the data bus. The data scanner also includes a switch network coupled to the row buffer. The switch network converts digital data received from the row buffer to analog data. This conversion is made using column load capacitances on pairs of column lines of the LCD. Similarly, Claim 10 is a method for driving

an LCD and includes the step of converting digital data to analog data. Again, this conversion of data is made using column load capacitances on pairs of column lines of the LCD.

The present disclosure eliminates the need for specific switched capacitor digital-to-analog converters and their associated amplifiers. The column line capacitances 160 (FIG. 4) are used along lines 135 to convert a digital signal to an analog signal.

Row buffer 110 distributes digital data arriving from bus 130 to switches 410 on a pulse received from a clock 120. The switches 410 convert the data using capacitance 160 shown in FIG. 4. See Applicant's specification at page 5, line 25 through page 6, line 5, and at FIG. 4.

b. Discussion of Edwards

Edwards does not disclose or suggest a switch network that converts digital data received from the row buffer to analog data by using column load capacitances on pairs of column lines of the LCD. Edwards discloses at page 2 that a liquid crystal display includes a row and a column of picture elements. The picture elements 12 include switching TFTs 16, which are connected to sets of conductors 18 and 19.

The picture elements are formed from display elements that are located on electrodes carried by opposing surfaces of first and second substrates. See Edwards at paragraph 21.

Drive signals for driving the picture elements are supplied from a peripheral drive circuit, and switching waveforms are applied by timing circuits. Edwards discloses at paragraphs 22-25, that charge sharing occurs between two halves of the column capacitance, or along a length of the column conductor electrode 19 as shown in FIG. 2. Edwards also teaches at page 1, paragraph 3, a charge of a capacitor element, which is divided into two sub-capacitor elements is shared.

There is no disclosure in Edwards of converting digital data received from the row buffer to analog data using column load capacitances on pairs of column lines of the LCD. For this limitation, the Office is looking to the secondary reference, Sekine.

c. Discussion of Sekine

Sekine describes a problem with a conventional Digital to Analog Converter for a TFT data driver shown in FIG. 1. Sekine describes that by using a conventional Digital to Analog converter (1) the output is problematically supplied directly to the signal lines and, thus, the output voltage is lower than the voltage normally applied to a capacitor array. Secondly, by using a conventional Digital to Analog converter and (2) by raising the resolution of the Digital to Analog Converter, then this resolution increase also results in an increase in the circuit area, which is problematic. See Sekine at page 1, paragraphs 5-6.

Sekine discloses a liquid crystal display that includes a pixel matrix, a data driver 20 for driving signal lines, and gate drivers 40_1 and 40_2. The gate drivers drive the scanning lines that are connected to the gate terminals. The pixel matrix includes pixel TFTs, which are active elements for each pixel. The matrix also has a liquid crystal capacitance, and a storage capacitance that are connected to the pixels TFTs.

In the matrix, one signal line is arranged for each pixel column and two scanning lines are arranged for each row. One scanning line is connected to the odd numbered pixel columns and the other scanning line is connected to even numbered pixel columns. See Sekine at page 3, paragraph 51.

The serial digital analog conversion circuits are provided in the data driver 20. See Sekine at the Abstract of the disclosure. Each serial digital analog conversion circuit 10_1 to 10_4 is provided for two adjacent signal lines.

d. Non-obviousness Analysis

In the Action at page 2, the Office contends that Sekine discloses "the concept of converting digital data to analog data using column load capacitances on pairs of column lines of the LCD (see the abstract; paragraphs [0016] and [0054])." The Examiner is erroneous. Neither Edwards, or Sekine disclose or suggest a switch network that converts digital data received from the row buffer to analog data using column load capacitances on pairs of column lines of the LCD.

Sekine uses two row lines per row of pixels to convert the digital data received from the row buffer to analog data, not by using column load capacitances on pairs of column lines of the LCD. Put simply, Sekine includes two pixels that are included in the same pixel row that are each connected to mutually different scanning row lines. Sekine does not disclose or suggest using the column load capacitances on pairs of column lines of the LCD. One of ordinary skill in the art would not be motivated to alter Sekine to use the pairs of column lines of the LCD after reviewing Sekine. Moreover, the Office is using impermissible hindsight reconstruction analysis to render the Claims obvious.

Sekine does not cure the deficiencies of the primary reference. If Sekine were combined with the primary reference Edwards, the resulting combination would result in using different scanning row lines, and not using column load capacitances on pairs of column lines of the LCD.

There is no disclosure or suggestion in Sekine or Edwards either separately or in combination, of a switch network that converts digital data received from the row buffer to analog data using column load capacitances on pairs of column lines of the LCD.

Reconsideration and withdrawal of the rejection are respectfully requested. Claim 10 is patentable for reasons similar to those argued above for independent Claim 1. Claims 19-20 depend from Claim 1 and are patentable for at least the same reasons discussed above for Claim 1.

3. Rejection of Claims 2-8 and 11-17 under 35 U.S.C. § 103(a)

In the Action, Claims 2 through 8, and 11 through 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Edwards and Sekine in view of United States Published Patent Application No. 2002/0135557A1 to Janssen et al. (hereinafter "Janssen"). The Action states that Janssen is cited to show that, connecting a switching device to adjacent column lines 80A and 80B of an LCD wherein a first column of the pair is coupled to alternating pixels of the first column line, is "old."

Janssen discloses a multiplexer at FIG. 3 that is connected to column lines 80A and 80B of a liquid crystal display. Each column is split into two column lines, and by this "splitting of the column lines" the capacitance of each line is a fraction of that required by a single column,

and reduces the capacitance load on the columns. Sekine discloses using a capacitance of two rows.

Janssen does not remedy the deficiencies of Edwards or Sekine. Neither Edwards, Sekine, nor Janssen, separately or in any combination disclose or suggest converting digital data received from the row buffer to analog data using column load capacitances on pairs of column lines of the LCD, as in Applicant's Claims 1 and 10. Therefore, independent Claims 1 and 10 meet the requirements of 35 U.S.C. § 103(a), in view of Edwards, Sekine, and Janssen. Claims 2 through 8 are patentable, as these claims depend on Claim 1. Claims 11 through 17 are also patentable, as they depend from independent Claim 10. Reconsideration and withdrawal of the rejection of Claims 2-8, and 11-17 under 35 U.S.C. § 103(a) are requested.

4. Rejection of Claims 9 and 18 under 35 U.S.C. § 103(a)

In the Action, Claim 9 and 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Edwards, Sekine, and Janssen in view of United States Patent No. 5,619,225 to Hashimoto *et al.* (hereinafter "Hashimoto"). Specifically, the Office contends that Hashimoto discloses a delta layout pixel arrangement in FIGS. 4 and 5.

Hashimoto discloses at Column 2, line 64 through Column 3, line 6, that the unit of the pixel of the display element section 410 is formed of a switching transistor 411, and a pixel holding capacitance 412. The other terminal of the pixel holding capacitance 412 is connected to an electrode voltage V_{LC}. Color signals are sent from a processing circuit to a sampling circuit 430. In a control circuit 460, the necessary pulses are formed and are supplied to the vertical scanning circuit 420, the horizontal scanning circuit 440, and the signal processing circuit 450. Hashimoto further discloses that the signal processing circuit is connected to an amplifier 480 in FIG. 20.

Hashimoto does not remedy the deficiencies of the cited references, and does not disclose or suggest converting digital data received from the row buffer to analog data using column load capacitances on pairs of column lines of the LCD as claimed in Claim 1. Claim 9 and 18 depend from independent Claims 1 and 10, respectively.

None of the cited references, taken separately or in combination, disclose or suggest Applicant's claimed invention as set forth in dependent Claims 9 and 18. Reconsideration and

withdrawal of the rejection of Claims 9 and 18 under 35 U.S.C. § 103(a) are respectfully requested.

5. New Claim 21.

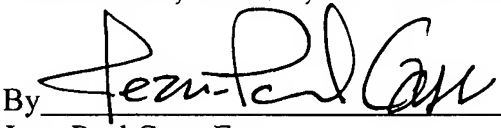
Applicant respectfully submits that none of the references disclose or suggest a switch network converts digital data received from the row buffer to analog data using column load capacitances on adjacent pairs of column lines of the LCD. Support for new Claim 21 can be found at various locations of the Applicant's specification, for example at FIG. 4, and at page 5, line 25 to page 6, line 4. Allowance of Claim 21 is respectfully requested.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By 

Jean-Paul Cass, Esq.
Registration No.: 46,605
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

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